In the Claims:

1. (currently amended) A method of manufacturing a semiconductor device, comprising:

providing a substrate;

placing a gate structure having a gate sidewall spacer over said substrate;

creating a halo implant in said substrate on opposing sides of said gate structure;

introducing a compensation implant in said substrate proximate said halo implant at an angle abnormal to said substrate; and

forming a source/drain region proximate said compensation implant, said angle reducing a capacitance associated with said halo implant or said source/drain region.

2. (currently amended) The method as recited in Claim 1 wherein the step of introducing a compensation implant includes introducing a compensation implant at an angle from about 5 degrees to about 75 degrees relative to normal of said substrate.

3. (currently amended) The method as recited in Claim 1 ~~2~~ wherein the step of introducing a compensation implant ~~at an angle from about 5 degrees to about 75 degrees relative to normal of said substrate~~ includes introducing a compensation implant at an angle from about 15 degrees to about 35 degrees relative to normal of said substrate.

4. (currently amended) The method as recited in Claim 1 wherein said compensation implant extends from beneath the footprint of said gate sidewall spacer toward and under said source/drain region ~~introducing a compensation implant includes introducing a compensation implant using a dopant dose ranging from about 1E13 atoms/cm^2 to about 1E14 atoms/cm^2~~.

5. (previously presented) The method as recited in Claim 1 wherein said compensation implant forms a dopant gradient between said halo implant and said source/drain region, thereby reducing said capacitance.

6. (currently amended) The method as recited in Claim 1 wherein said steps of introducing and ~~said~~ forming includes introducing and forming using a similar type dopant and said creating includes creating using an opposite type dopant.

7. (previously presented) The method as recited in Claim 1 wherein said source/drain region includes a lightly doped source/drain implant and a heavily doped source/drain implant.

8. (currently amended) The method as recited in Claim 1 further including the step of forming gate sidewall spacers along sides of said gate structure, wherein said compensation implant is located at least about 10 nm under a footprint created by said gate sidewall spacers.

9. (previously presented) The method as recited in Claim 8 wherein said compensation implant is located from about 10 nm to about 200 nm under said footprint created by said gate sidewall spacers.

10. (currently amended) The method as recited in Claim 1 wherein said step of creating occurs before said introducing and said introducing occurs before said forming.

11. (previously presented) The method as recited in Claim 1 wherein introducing a compensation implant includes creating a counterdoped region in said halo implant.

12. (currently amended) The method as recited in Claim 11 wherein said counterdoped region has a dopant concentration greater than about 1/3 of a dopant concentration of said halo implant.

13. (currently amended) The method as recited in Claim 1 wherein the stop of introducing a compensation implant includes introducing a first compensation implant and further including introducing a second compensation implant in said substrate proximate said halo implant at an angle substantially normal to said substrate.

14. (currently amended) The method as recited in Claim 13 wherein said steps of introducing a first compensation implant and said introducing a second compensation implant occur simultaneously.

15. (previously presented) A semiconductor device manufactured by the method of Claim 1.

16. (currently amended) A method of manufacturing an integrated circuit, comprising:

creating a semiconductor device, including;

providing a substrate;

placing a gate structure over said substrate having sidewalls;

creating a halo implant in said substrate on opposing sides of said gate structure;

introducing a compensation implant in said substrate proximate said halo implant at an angle abnormal to said substrate; and

forming a source/drain region proximate said compensation implant, said angle reducing a capacitance associated with said halo implant or said source/drain region; and

constructing an interlevel dielectric layer located over said semiconductor device and having interconnects located therein, wherein said interconnects contact said semiconductor device to form an operational integrated circuit.

17. (currently amended) The method as recited in Claim 16 wherein the step of introducing a compensation implant includes introducing a compensation implant at an angle from about 15 degrees to about 35 degrees relative to normal of said substrate.

18. (currently amended) The method as recited in Claim 16 wherein said compensation implant extends from beneath the footprint of said gate sidewall spacer toward and under said source/drain region ~~introducing a compensation implant includes introducing a compensation implant using a dopant dose ranging from about 1E13 atoms/cm^2 to about 1E14 atoms/cm^2~~.

19. (currently amended) The method as recited in Claim 16 wherein said steps of introducing and said forming includes introducing and forming using a similar type dopant and said creating includes creating using an opposite type dopant.

20. (previously presented) The method as recited in Claim 16 wherein said source/drain region includes a lightly doped source/drain implant and a heavily doped source/drain implant.

21. (currently amended) The method as recited in Claim 16 further including the step of forming gate sidewall spacers along sides of said gate structure, wherein said compensation implant is located at least about 10 nm under a footprint created by said gate sidewall spacers.

22. (previously presented) The method as recited in Claim 1 wherein introducing a compensation implant includes creating a counterdoped region in said halo implant.

23. (currently amended) The method as recited in Claim 22 ~~1~~ wherein said counterdoped region has a dopant concentration greater than about 1/3 of a dopant concentration of said halo implant.

24. (currently amended) The method as recited in Claim 1 wherein the steps of introducing a compensation implant includes introducing a first compensation implant and further including introducing a second compensation implant in said substrate proximate said halo implant at an angle substantially normal to said substrate.

25. (currently amended) The method as recited in Claim 24 wherein said steps of introducing a first compensation implant and said introducing a second compensation implant occur simultaneously.

26. (currently amended) The method as recited in Claim 16 further including the step of forming a second semiconductor device proximate said semiconductor device, wherein said second semiconductor device is selected from the group of devices consisting of:

a MOS device;

a bipolar device;

an inductor;

a resistor;

an optical device; and

a micro-electro-mechanical system (MEMS) device.

27. (currently amended) A semiconductor device, comprising;

a substrate having a gate structure located thereover;

sidewall spacers located along sides of said gate structure;

a halo implant located in said substrate on opposing sides of said sidewall spacers;

a compensation implant located in said substrate proximate said halo implant and at least about 10 nm under a footprint created by said gate sidewall spacers; and

a source/drain region located proximate said compensation implant.

28. (previously presented) The semiconductor device as recited in Claim 19 wherein said compensation implant is located from about 10 nm to about 200 nm under said footprint created by said gate sidewall spacers.